

MS-AA711 Ver: 2.2

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CPU:

INTEL - Ivy bridge LGA1155

System Chipset:

INTEL-Cougar Point (H61)

OnBoard Chipset:

HD Audio Codec:ALC887

LAN:Realtek RTL8111E

SIO:Nuvoton NCT6681D

USB3.0:ASMedia ASM1042

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

MINIPCI Express (X1) Slot * 2

PWM:

Controller:NCP6131 3 + 1 Phase (65W)

Other:

SATA(SATA2-300MB/s) *2

USB2.0 *4

USB3.0 *2

HDMI OUT*1

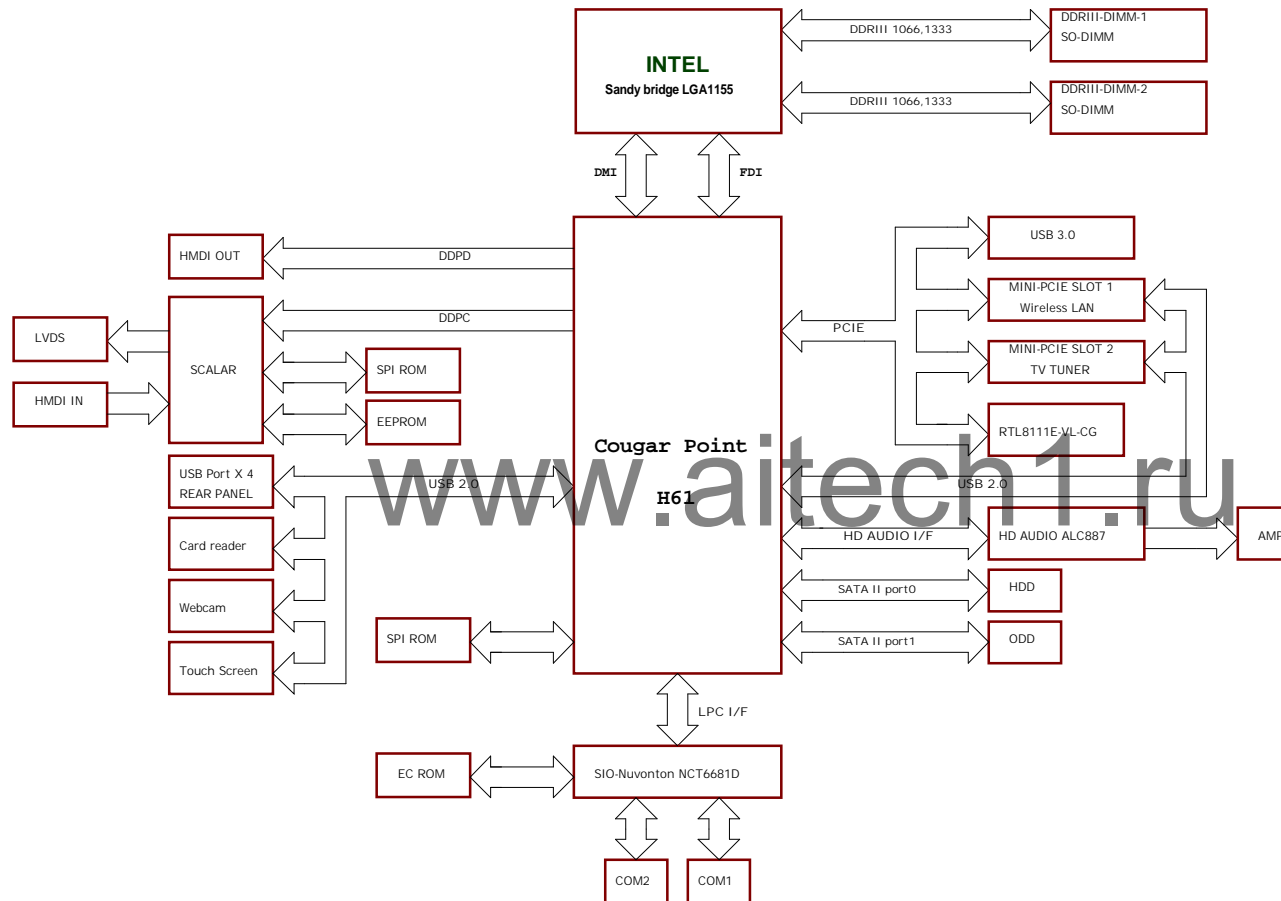
HDMI IN*1

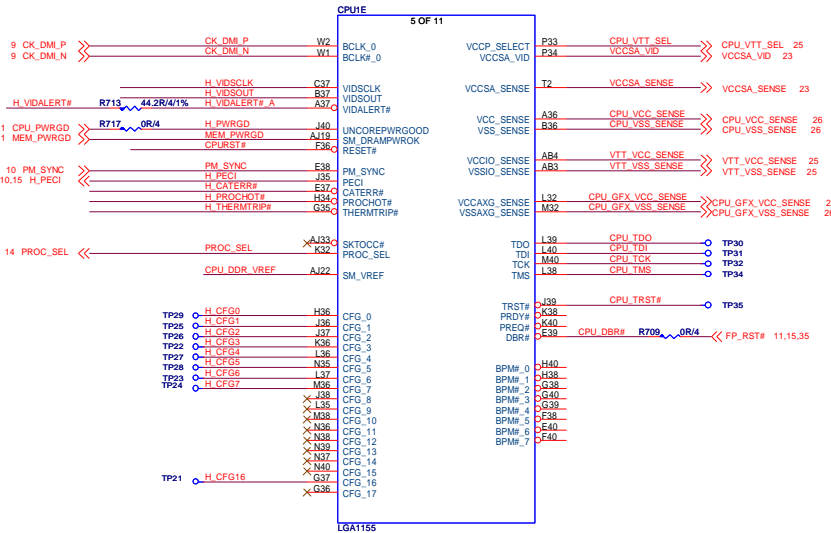
Card reader*1

COM Port*2

MS-AA711

Ver: 2.2

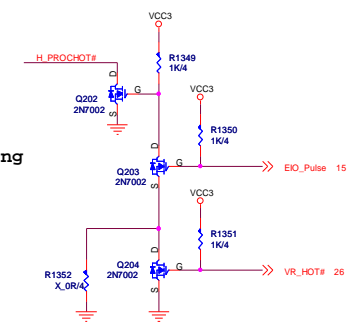
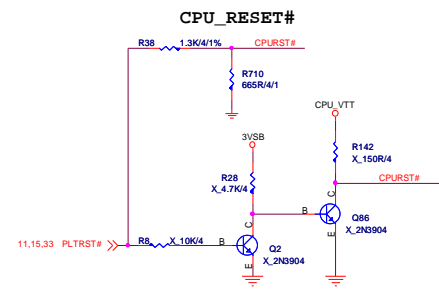
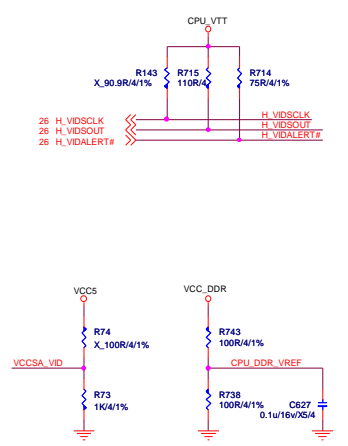
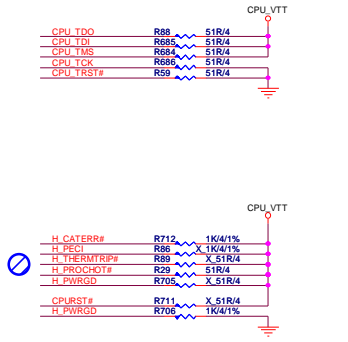
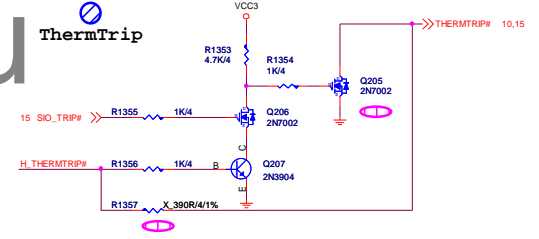
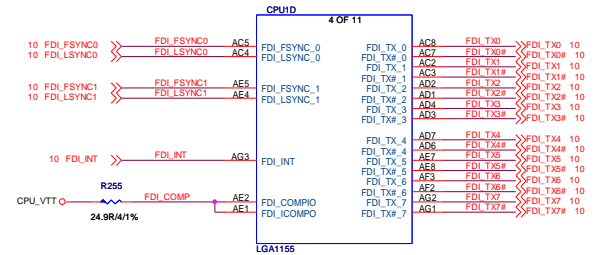




N12-155A020-L06

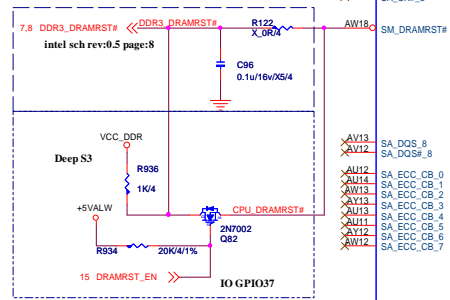
Break-out: 10mil width, 6 mil space
Other Area: 10mil width, 15 mil space

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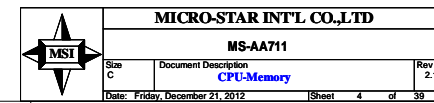


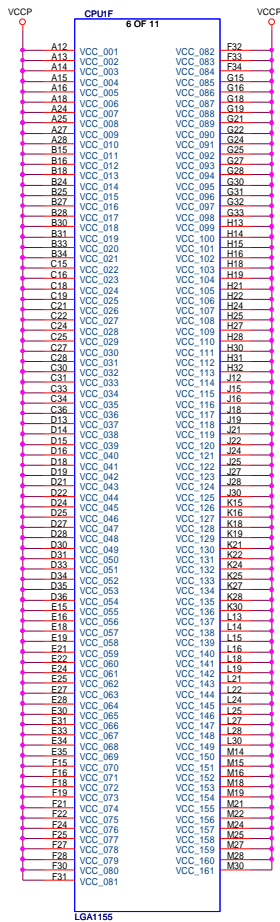
PEG CONFIG TABLE

SEL2	SEL1	SEL0	PCI CONFIG
1	1	1	1 X 16
1	1	0	2 X 8



ATA45	8 MEM_MB_CLK_H0	MEM_MB_CLK_H0	AL220	SB_CLK_0
ATA46	8 MEM_MB_CLK_L0	MEM_MB_CLK_L0	AL221	SB_CLK_0
ATA47	8 MEM_MB_CLK_H1	MEM_MB_CLK_H1	AK200	SB_CLK_1
ATA48	8 MEM_MB_CLK_L1	MEM_MB_CLK_L1	AK201	SB_CLK_1
ATA49			AK202	SB_CLK_2
ATA50			AK203	SB_CLK_2
ATA51			AK204	SB_CLK_3
ATA52			AK205	SB_CLK_3
ATA53			AK206	SB_CLK_3
ATA54			AK207	SB_CLK_3

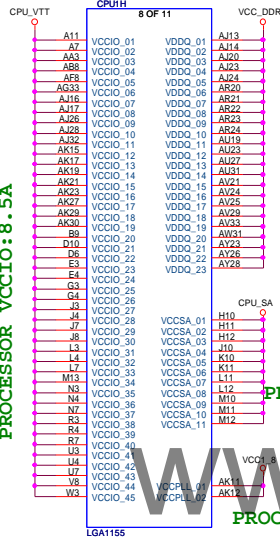




MSI N12-155A020-L06

PROCESSOR VDDQ:4.75A

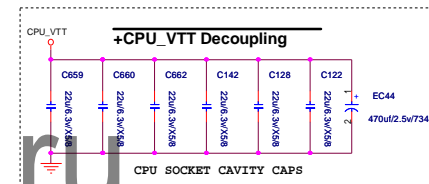
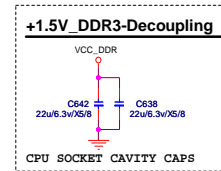
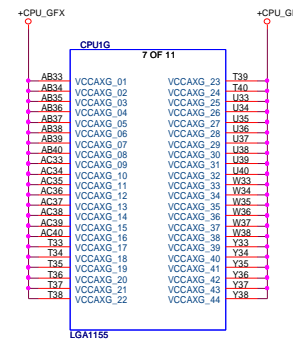
PROCESSOR VCCIO:8.5A



PROCESSOR VCCSA:8.8A

PROCESSOR VCCPLL:1.5A

PROCESSOR VAXG:35A



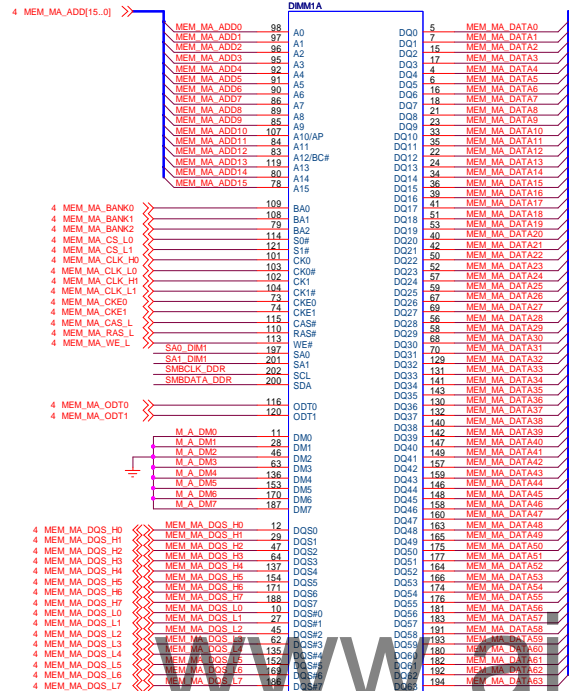
MICRO-STAR INT'L CO.,LTD

MS-AA711

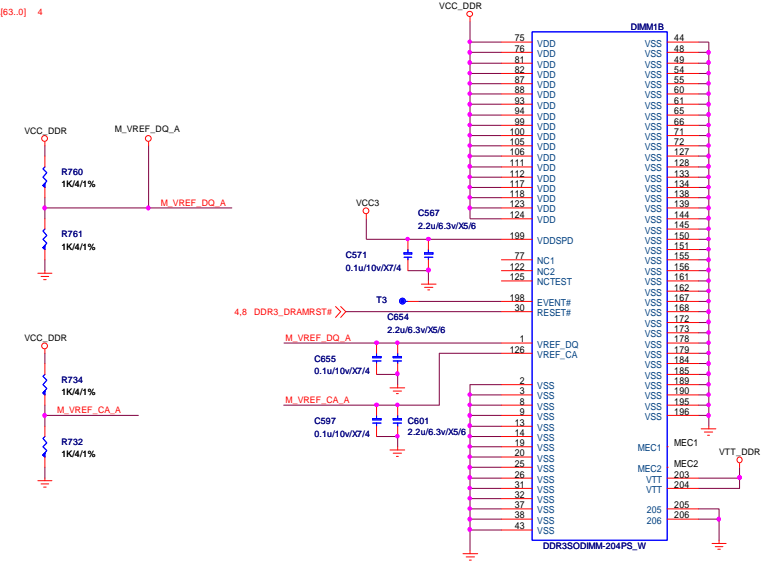
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SODIMM#A

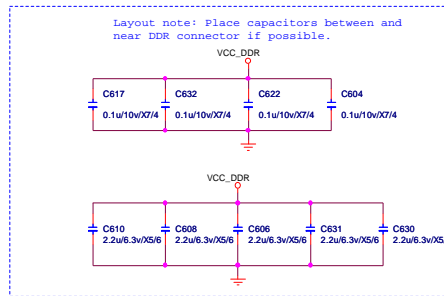


ADDRESS: 000
0xA0

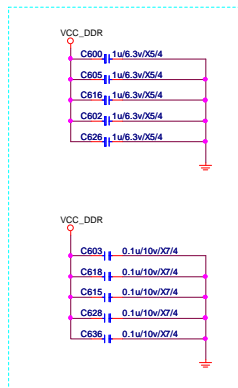
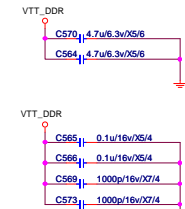


N13-2040790-CK3
H=5.2mm

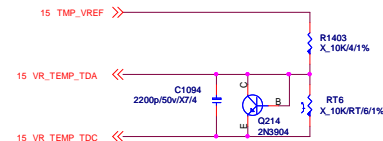
N13-2040800-CK3
H=9.2mm



CHANNEL A V_SM_VTT DECOUPLING CAPS



Temp. Sensor



SODIMM#B

4 MEM_MB_ADD[15:0]

MEM_MB_ADD0 98 A0
MEM_MB_ADD1 97 A1
MEM_MB_ADD2 96 A2
MEM_MB_ADD3 95 A3
MEM_MB_ADD4 94 A4
MEM_MB_ADD5 91 A5
MEM_MB_ADD6 90 A6
MEM_MB_ADD7 86 A7
MEM_MB_ADD8 89 A8
MEM_MB_ADD9 85 A9
MEM_MB_ADD10 107 A10/AP
MEM_MB_ADD11 84 A11
MEM_MB_ADD12 83 A12/BC#
MEM_MB_ADD13 118 A13
MEM_MB_ADD14 80 A14
MEM_MB_ADD15 78 A15

4 MEM_MB_BANK0
4 MEM_MB_BANK1
4 MEM_MB_BANK2
4 MEM_MB_CS_L0
4 MEM_MB_CS_L1
4 MEM_MB_CLK_H0
4 MEM_MB_CLK_L0
4 MEM_MB_CLK_H1
4 MEM_MB_CLK_L1
4 MEM_MB_CKE0
4 MEM_MB_CKE1
4 MEM_MB_CAS_L
4 MEM_MB_RAS_L
4 MEM_MB_WE_L

MEM_MB_BANK0 109 BA0
MEM_MB_BANK1 108 BA1
MEM_MB_BANK2 79 BA2
MEM_MB_CS_L0 114 S0#
MEM_MB_CS_L1 101 S1#
MEM_MB_CLK_H0 103 CK0#
MEM_MB_CLK_L0 102 CK0#
MEM_MB_CLK_H1 104 CK1#
MEM_MB_CLK_L1 102 CK1#
MEM_MB_CKE0 74 CKE0
MEM_MB_CKE1 115 CKE1
MEM_MB_CAS_L 110 CAS#
MEM_MB_RAS_L 113 RAS#
MEM_MB_WE_L 197 WE#
SA0_DM2 201 SA0
SA1_DM2 202 SA1
SCL 200 SCL
SDA 201 SDA
ODT0 116 ODT0
ODT1 120 ODT1

4 MEM_MB_DQS_H0
4 MEM_MB_DQS_H1
4 MEM_MB_DQS_H2
4 MEM_MB_DQS_H3
4 MEM_MB_DQS_H4
4 MEM_MB_DQS_H5
4 MEM_MB_DQS_H6
4 MEM_MB_DQS_H7
4 MEM_MB_DQS_H8
4 MEM_MB_DQS_H9
4 MEM_MB_DQS_L0
4 MEM_MB_DQS_L1
4 MEM_MB_DQS_L2
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4 MEM_MB_DQS_L5
4 MEM_MB_DQS_L6
4 MEM_MB_DQS_L7

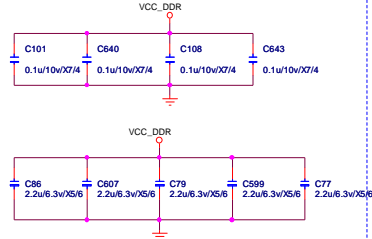
MEM_MB_DQS_H0 12 DQS0
MEM_MB_DQS_H1 29 DQS1
MEM_MB_DQS_H2 47 DQS2
MEM_MB_DQS_H3 64 DQS3
MEM_MB_DQS_H4 137 DQS4
MEM_MB_DQS_H5 154 DQS5
MEM_MB_DQS_H6 171 DQS6
MEM_MB_DQS_H7 188 DQS7
MEM_MB_DQS_H8 10 DQS8
MEM_MB_DQS_H9 27 DQS9
MEM_MB_DQS_L0 45 DQS10
MEM_MB_DQS_L1 62 DQS11
MEM_MB_DQS_L2 135 DQS12
MEM_MB_DQS_L3 152 DQS13
MEM_MB_DQS_L4 169 DQS14
MEM_MB_DQS_L5 186 DQS15
MEM_MB_DQS_L6 103 DQS16
MEM_MB_DQS_L7 120 DQS17

DDR3SODIMM-204P5_W

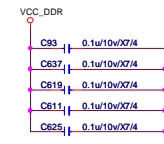
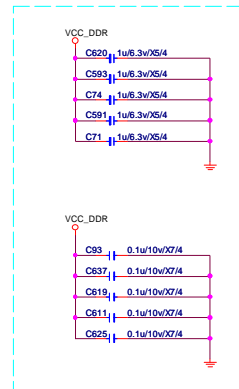
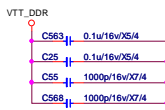
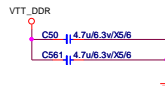
N13-2040790-CK3
H=5.2mm

ADDRESS: 010
0xA2

Layout note: Place capacitors between and near DDR connector if possible.



CHANNEL A V_SM_VTT DECOUPLING CAPS



N13-2040800-CK3
H=9.2mm

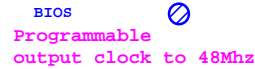


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H61 SKU:USB ports 6, 7, 12 and 13 are disabled.



XTAL_25M_PCH_OUT	AJ5	XTAL25_OUT	
XTAL_25M_PCH_IN	AJ3	XTAL25_IN	
CLKIN_GND1_P	P27	CLKIN_GND1_N	P27
CLKIN_GND1_N	P27	CLKIN_GND0_P	V52
CLKIN_GND0_P	V52	CLKIN_GND0_N	W53
CLK96M_DOT_P	BF38	CLK96M_DOT_N	B038
CLK100M_SATA_P	AG56	CLK100M_SATA_N	AF56
CLK100M_DMI1_P	R33	CLK100M_DMI1_N	P33
CK_148PM_PCH	AN8		

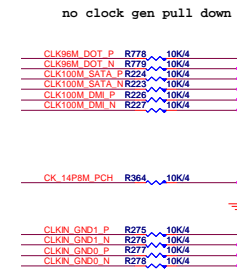
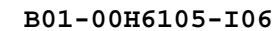
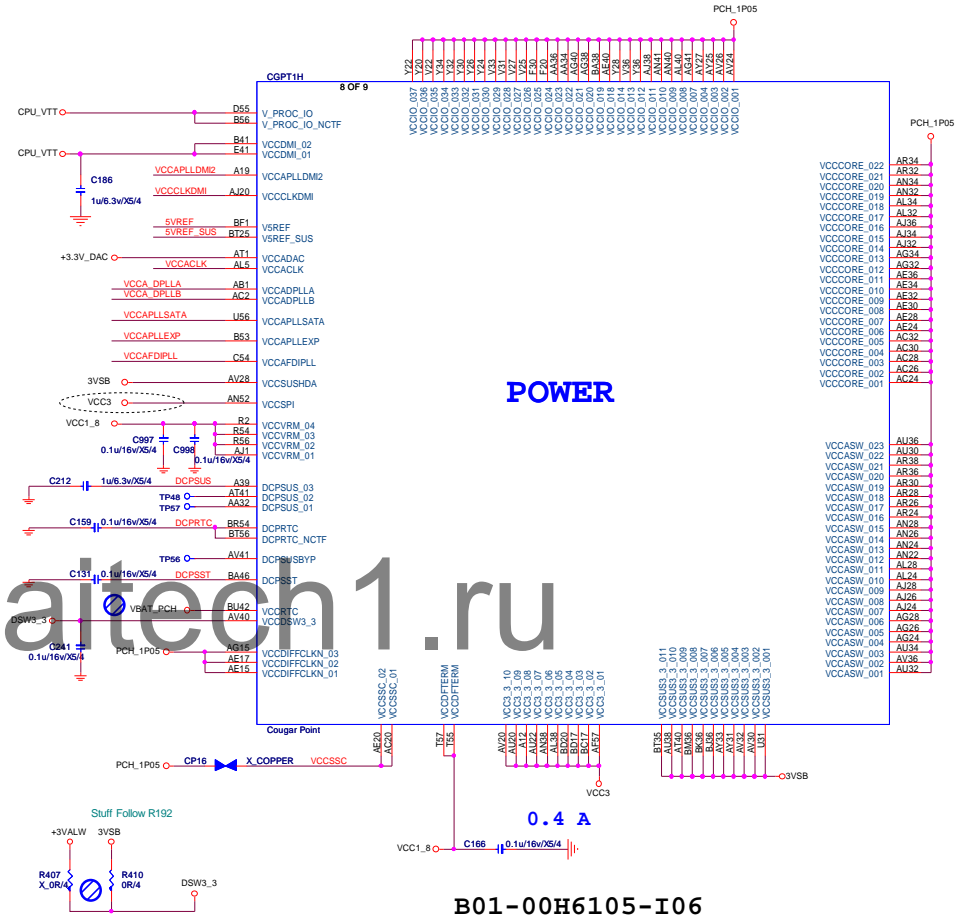
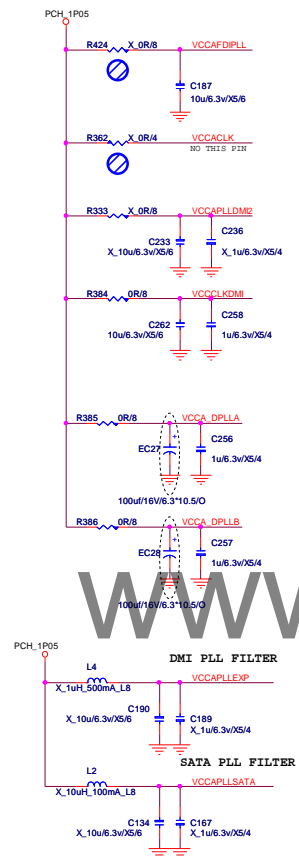
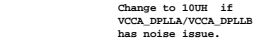
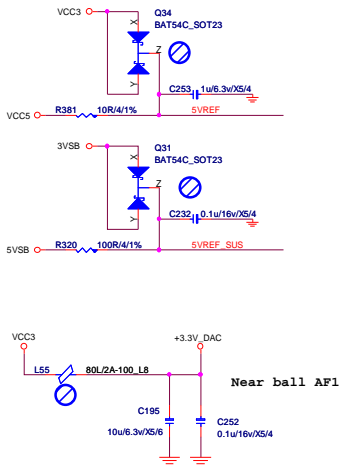


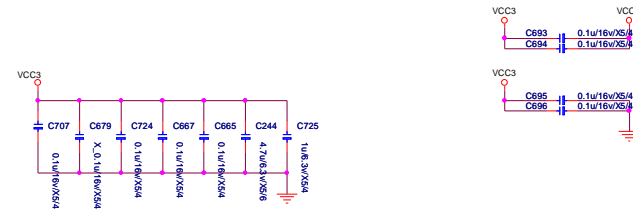
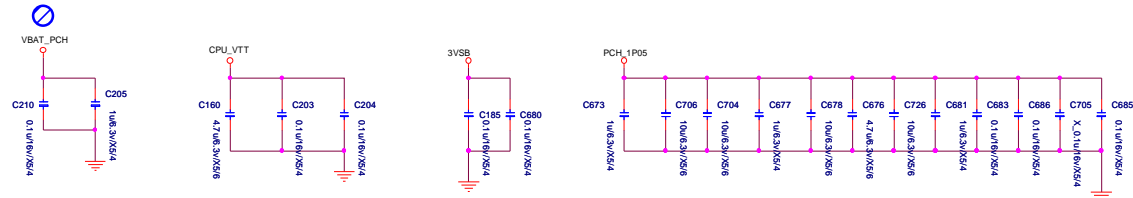
Table 3-7. VCCPLL Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Electrolytic 220µF	1	77mΩ	3.3nH	Output	North of processor - as close to RM keep-out as possible	1
10µF 0805 XSR	1	3mΩ	0.51nH	Output		1, 2, 3

5VREF & 5VREF_SUS Sequencing Circuit



PCH decoupling cap



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MS-AA711

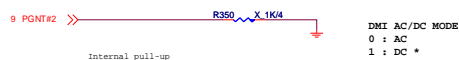
Size C	Document Description CP POWER
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CP REQUIRED STRAPS

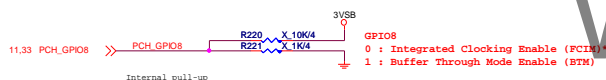
BOOT DEVICE	GNT0	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating



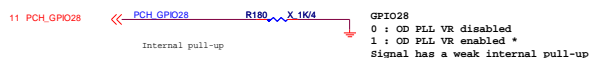
DMI AC/DC MODE
0 : AC
1 : DC *



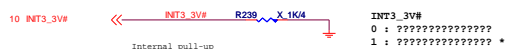
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (PCIe)
1 : Buffer Through Mode Enable (BTM)



GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ??????????????
1 : ?????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the
integrated GbS only operates at 10/100 Mbps during S3-S5.



DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V
regulators. Must beconnected even when not supporting DSW.



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

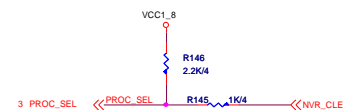


HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



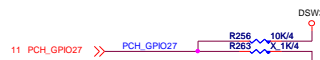
GEFO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



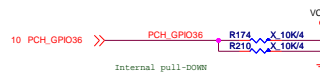
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



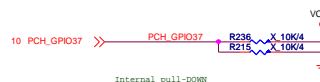
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



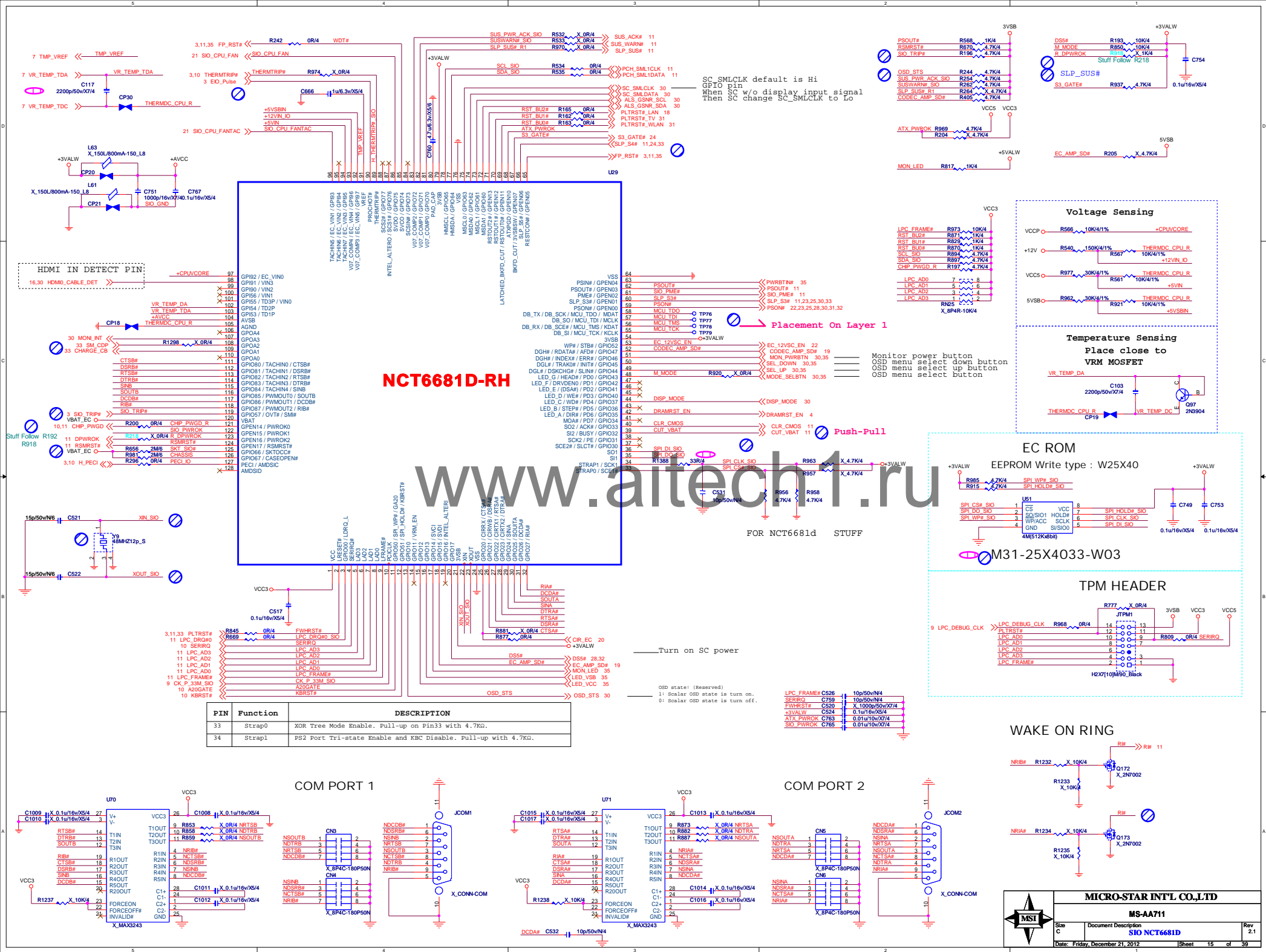
In Deep Sleep Power Well.
If not used,require a weak pull-up(8.2k-10k) to VccDSW3_3



Cougar point EDS PAGE:93 This signal should not be pull high

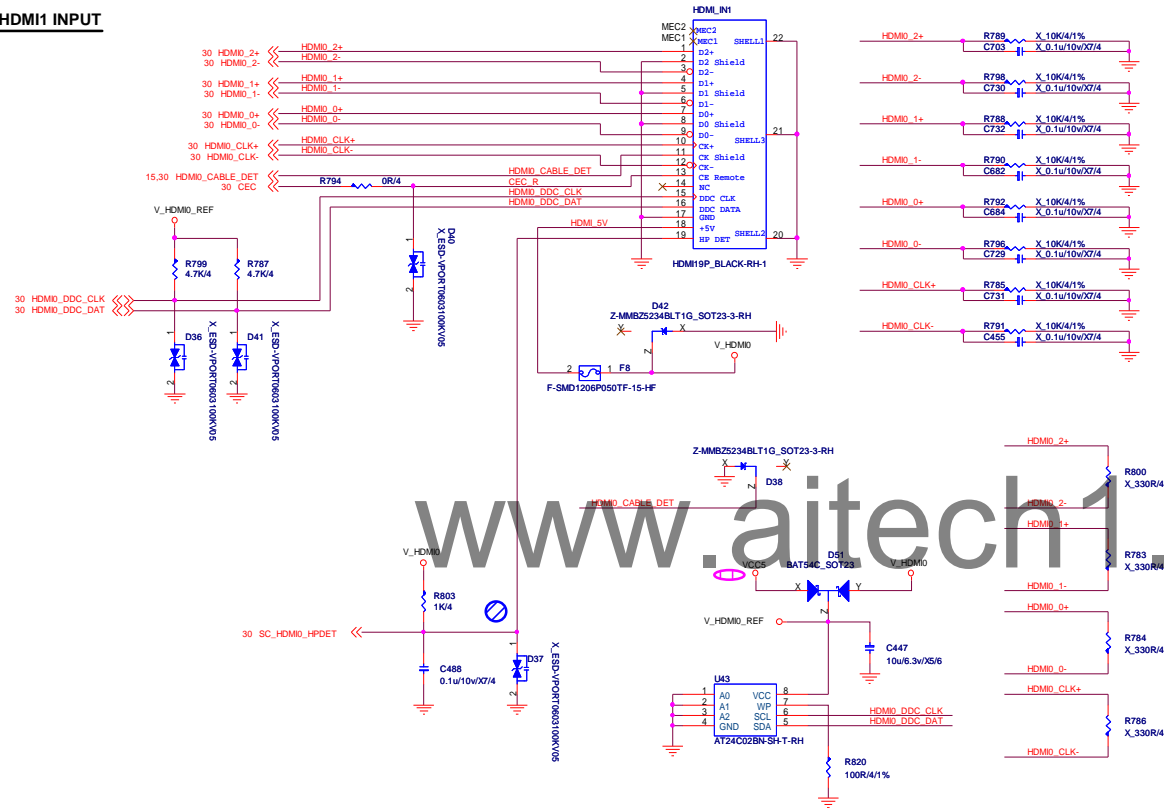


Cougar point EDS PAGE:93 This signal should not be pull high



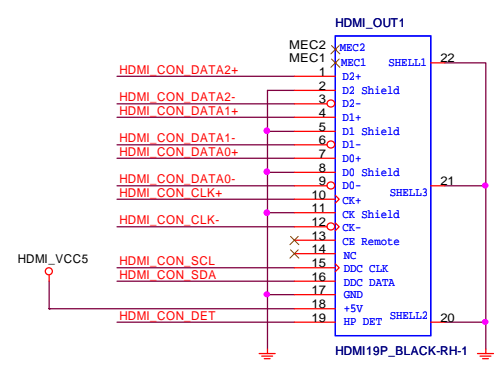
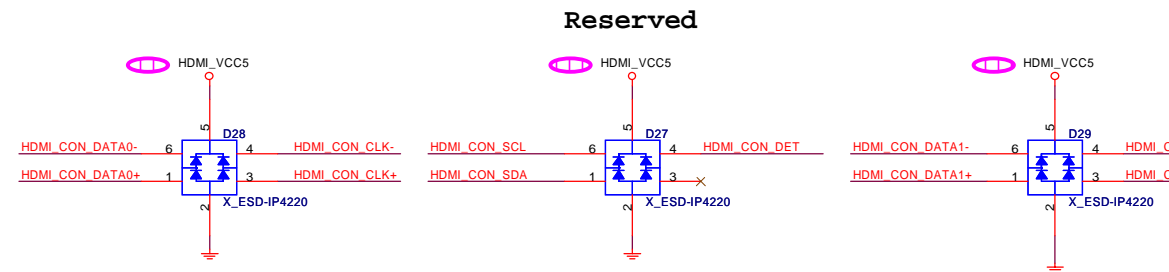
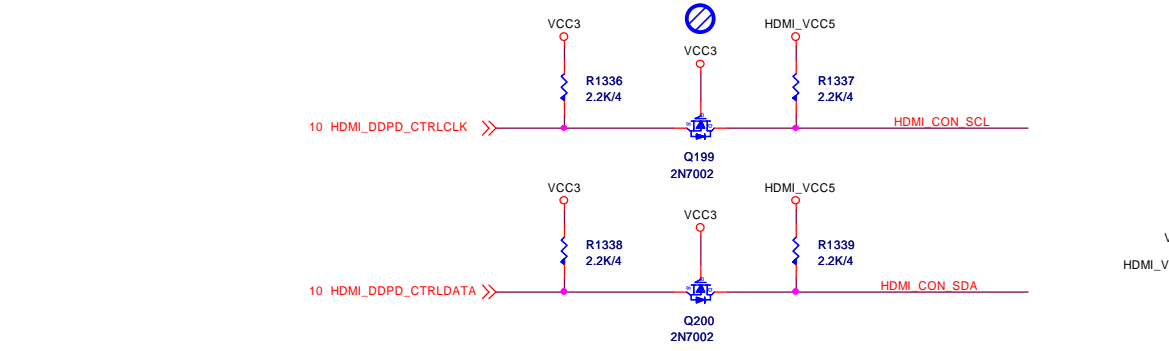
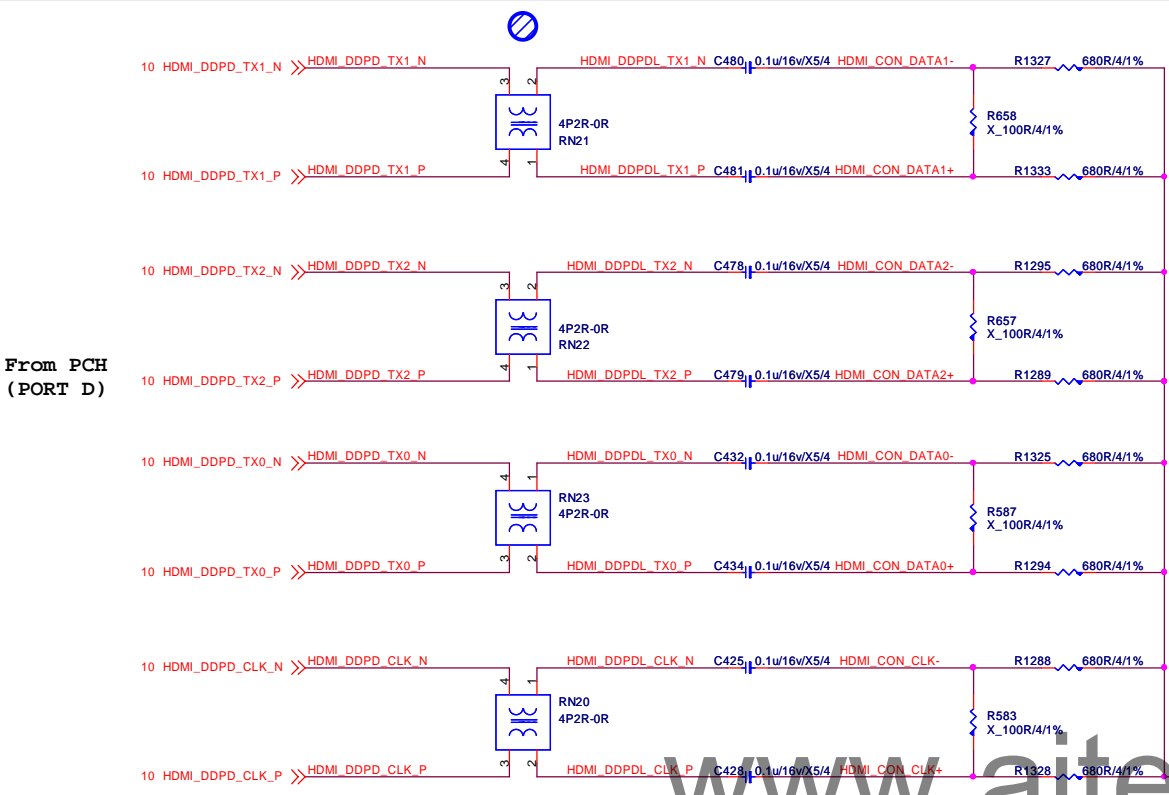
N5Y-19M0221-H06

HDMI INPUT

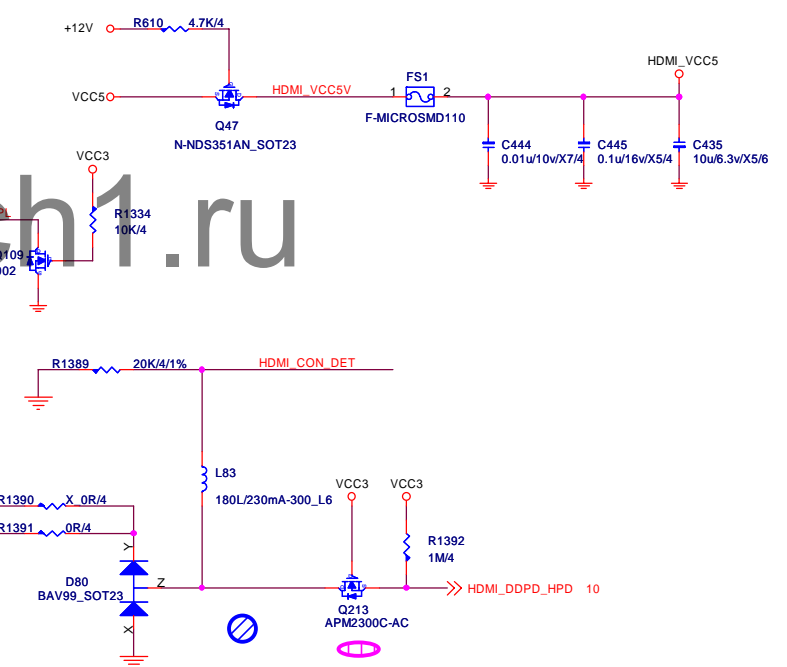


M33-24C02X3-A26

From PCH
(PORT D)



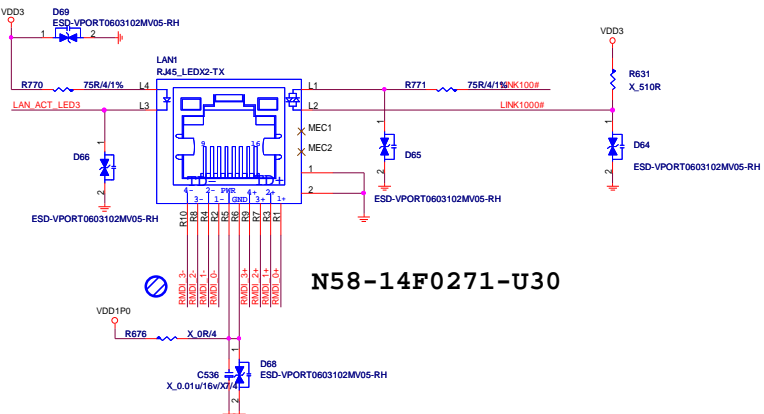
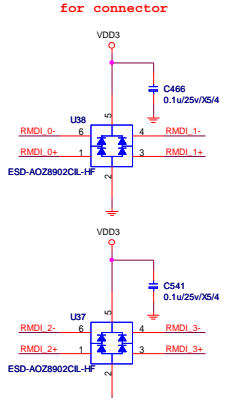
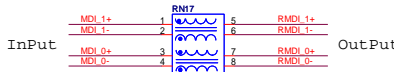
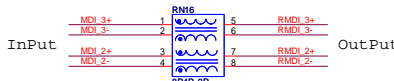
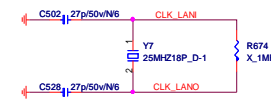
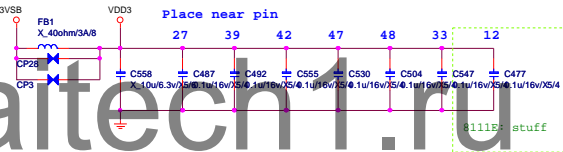
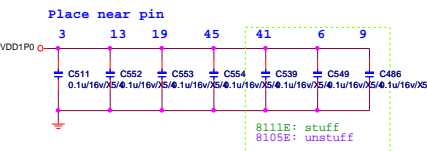
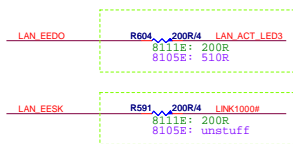
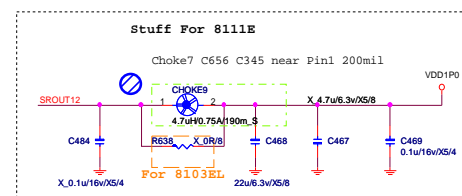
N5Y-19M0221-H06



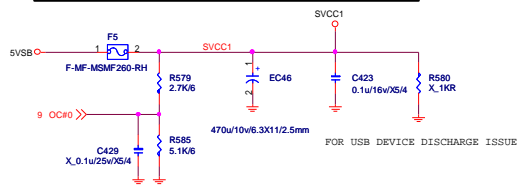
Symbol	Parameter	Test Conditions	APM2300CA			Unit
			Min.	Typ.	Max.	
Static Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	0.5	0.75	1	V



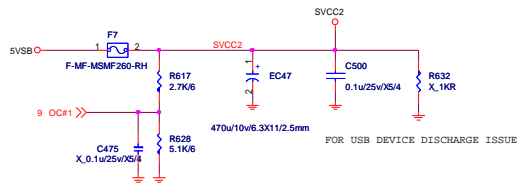
MICRO-STAR INT'L CO.,LTD			
MS-AA711			
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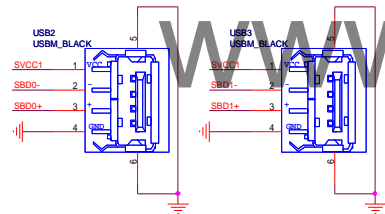
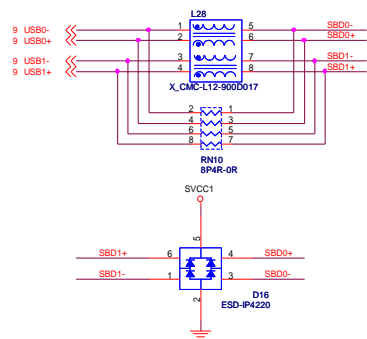
POWER CIRCUIT FOR USB PORT 0,1 (REAR)



POWER CIRCUIT FOR USB PORT 2,3 (REAR)

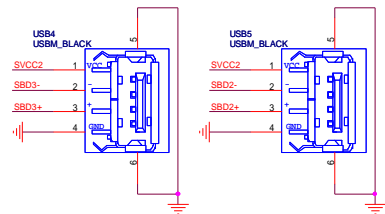
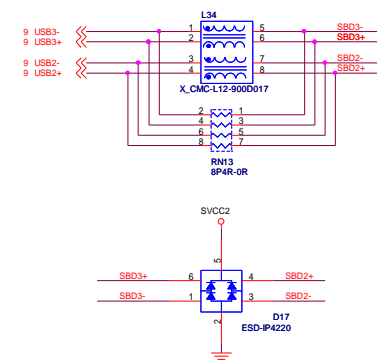


REAR PANEL USB CONNECTOR FOR USB PORT 0,1



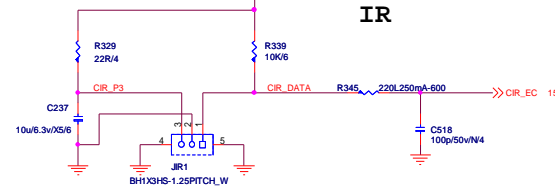
N53-04M0891-H06

REAR PANEL USB CONNECTOR FOR USB PORT 2,3



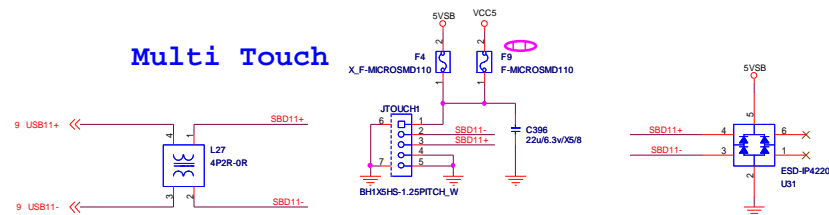
N53-04M0891-H06

Power consumption?



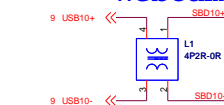
N32-1030130-H06

Multi Touch



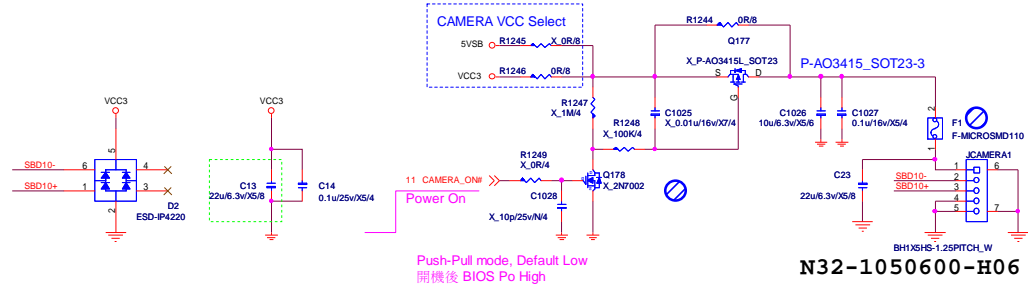
N32-1050600-H06

Webcam

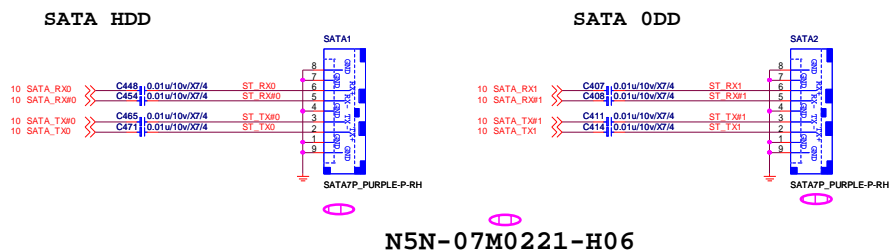


AO3415, AO3415L						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC PARAMETERS						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ $I_D=-250\mu A$	-0.3	-0.55	-1	

ViewSonic VCC5 (USB_STR2)



N32-1050600-H06

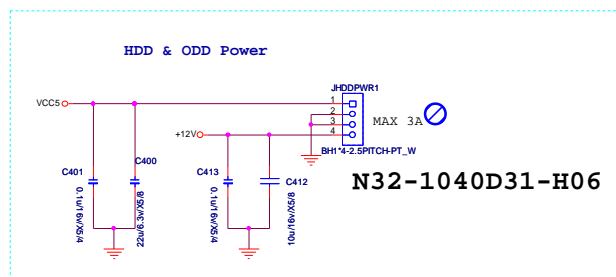
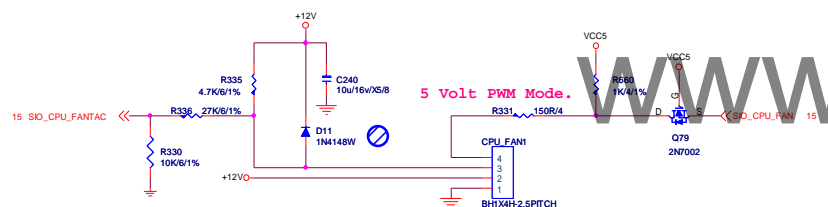


1.3 Intel® 6 Series Chipset and Intel® C200 Series Chipset SKU Definition

Table 1-2. Desktop Intel® 6 Series Chipset SKUs

Feature Set	SKU Name(s)						
	Q67	Q65	B65	Z68	H67	P67	H61
PCI Express® 2.0 Ports	8	8	8	8	8	8	6 ¹
PCI Interface	Yes	Yes	Yes	No ¹⁰	No ¹⁰	No ¹⁰	No ¹⁰
USB 2.0 Ports	14	14	12 ⁶	14	14	14	10 ⁷
Total number of SATA ports	6	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2 ⁴	1 ⁵	1 ⁵	2 ⁴	2 ⁴	2 ⁴	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4	4 ⁵
HDMI/DVI/VGA/DisplayPort®/eDP*	Yes	Yes	Yes	Yes	Yes	No	Yes
Integrated Graphics Support with PAVP	Yes	Yes	Yes	Yes	Yes	No	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes	No ³
	RAID 0/1/5/10 Support	Yes	No	No	Yes	Yes	No
Intel RST SSD Caching ¹¹	No	No	No	Yes	No	No	No
Intel® AT	Yes	Yes	No	No	No	No	No
Intel® AMT 7.0	Yes	No	No	No	No	No	No

CPU FAN



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CPU SA Power

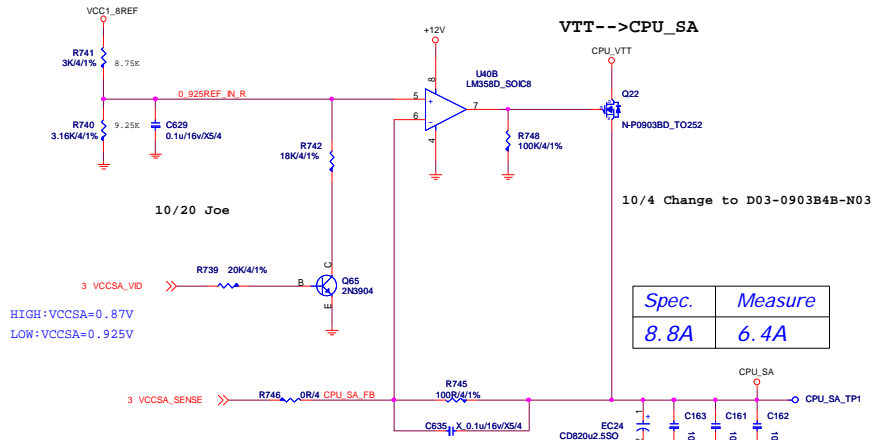
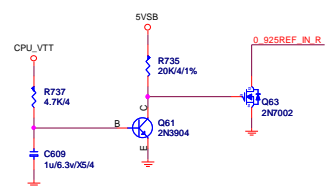


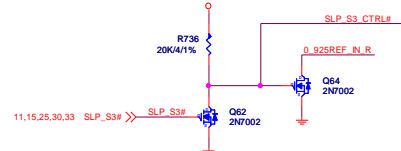
Table 3-10. VCCSA Decoupling Requirements

Capacitance	(V)	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 50uF	1	7mΩ	1.4nH	Output	As close to VM keep-out as possible	1
10uF 0805 50V	2	3mΩ	0.51nH	Output	Inside processor socket cavity	1,13

Waiting CPU_VTT Ready



CRB



CP Power

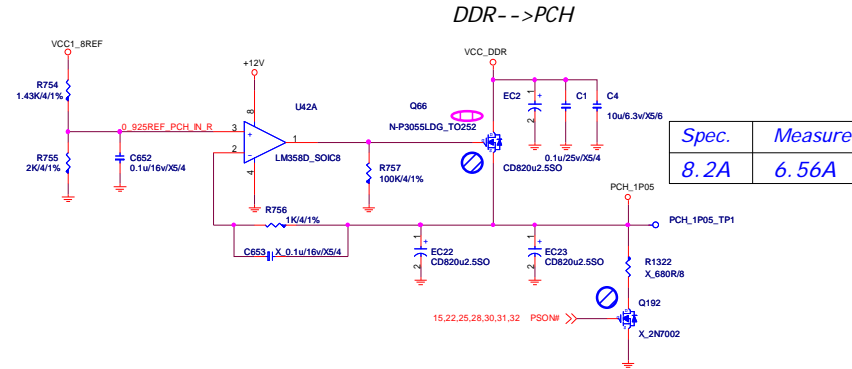
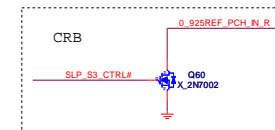


Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

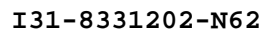
Bulk Decoupling Location	Qty x uF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated) (AMT sku)	1x820uF	21mohm (bulk)
1.05A rail for VccASW (dedicated) (AMT sku)	2x22uF MLCC	
1.05S rail merge with 1.05A rail (non- AMT sku)	1x560uF	7mohm (bulk)
	2x 22uF MLCC	

Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different than those shown.



C71-4702530-S03

DDR III 1.5V POWER

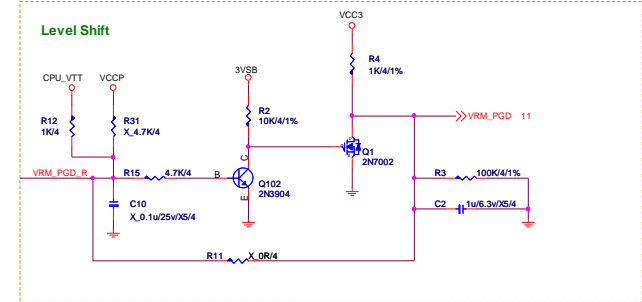
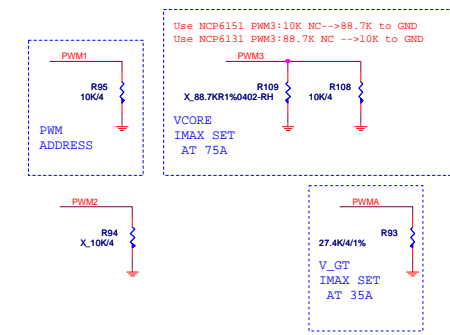
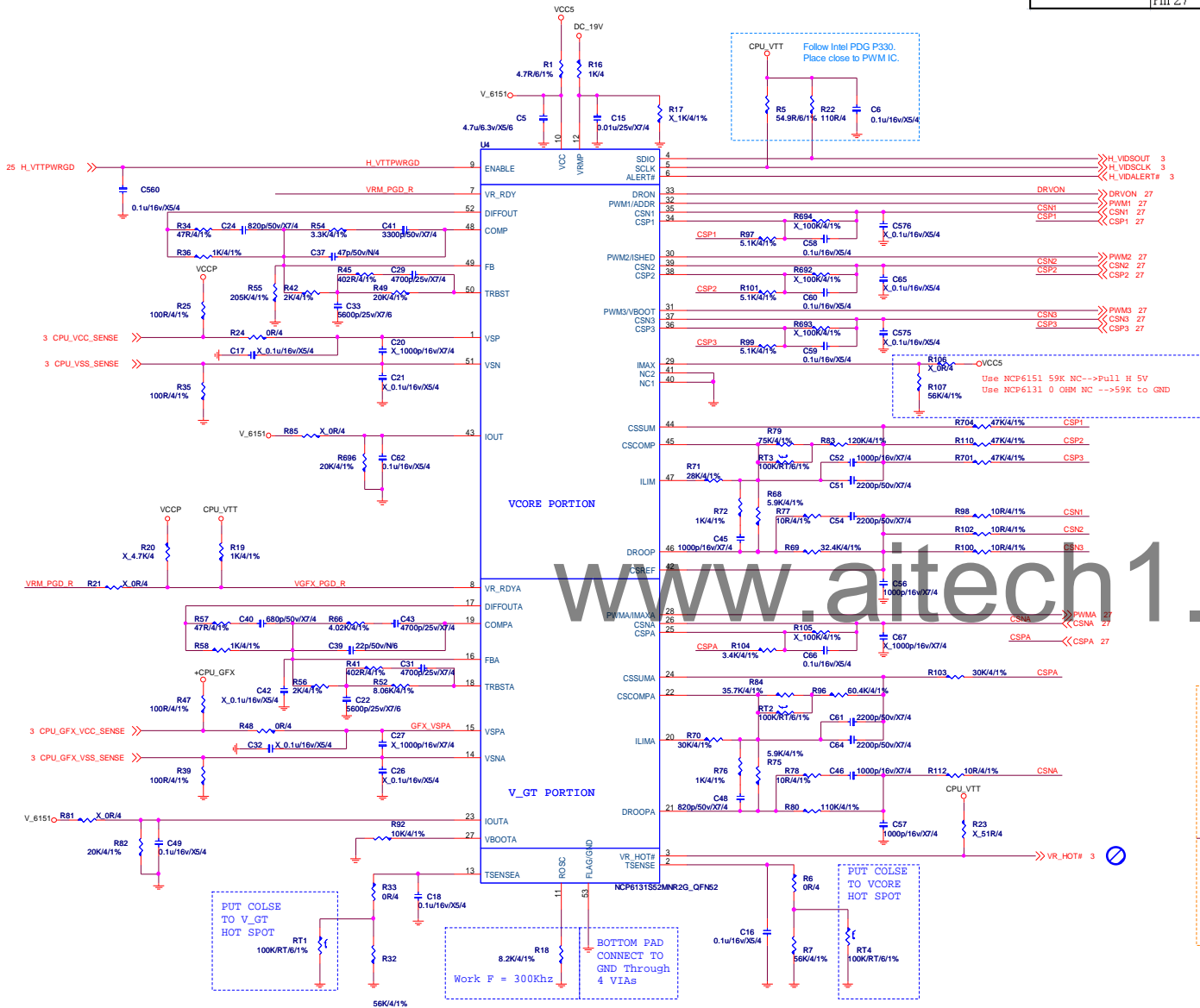


Modulize of NCP6151/NCP6131 COLAY (19V VR12)

PWM,ON Semiconductor/NCP6131S52MNR2G					
Without CPU Boot	Pin 31	VBOOT	R108	95K	SVID Address for VCORE Rail
	Pin 27	VBOOT	R92	95K	SVID Address for GFX Rail
					1000
					1001

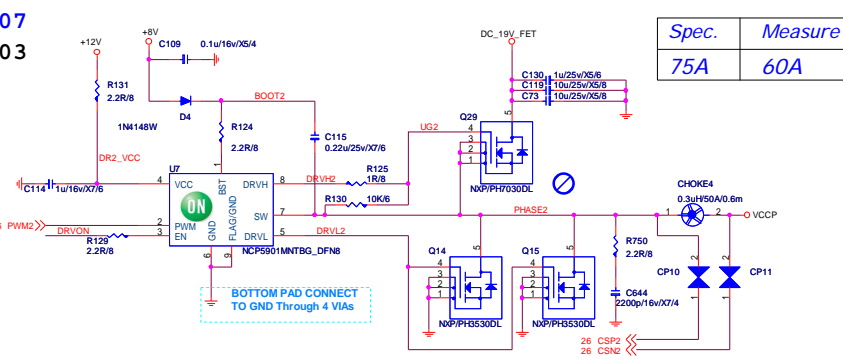
BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101



I32-6131S0C-O05

+CPU_VCCP



VCCP

VCCP_TP1

EC19 1+ (2 CD820u2 SSO)

EC18 1+ (2 CD820u2 SSO)

EC17 1+ (2 CD820u2 SSO)

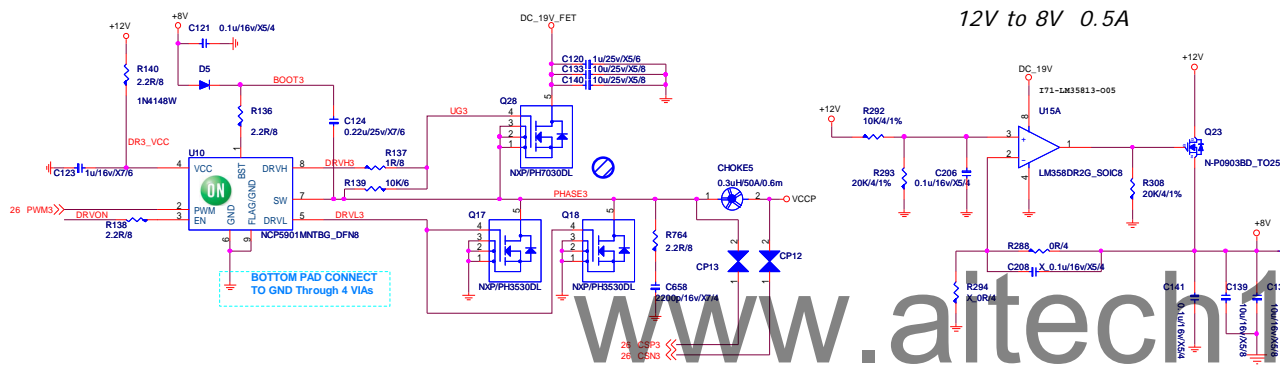
EC16 1+ (2 CD820u2 SSO)

EC13 1+ (2 CD820u2 SSO)

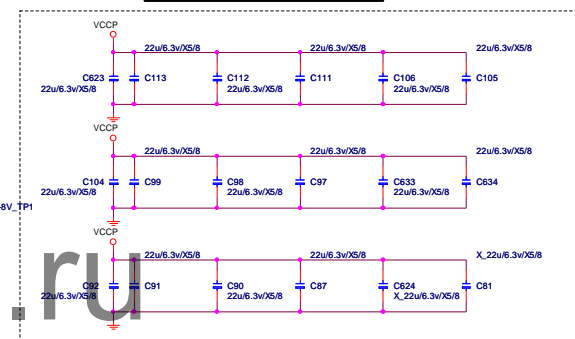
EC15 1+ (2 CD820u2 SSO)

EC14 1+ (2 CD820u2 SSO)

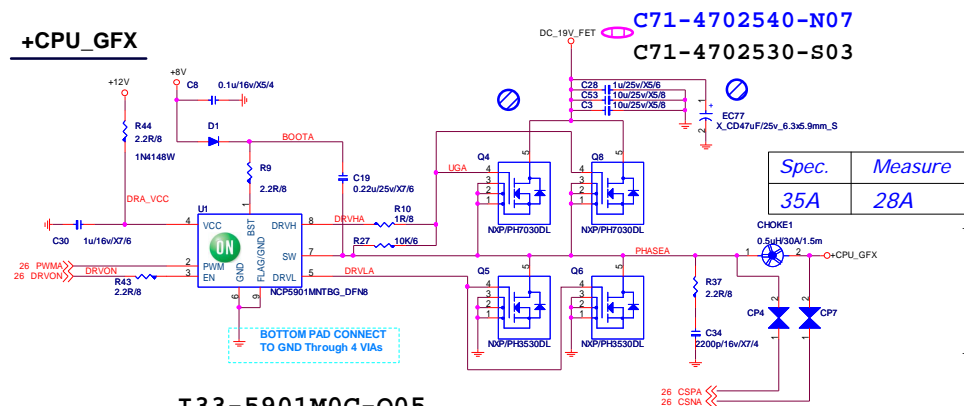
12V to 8V 0.5A



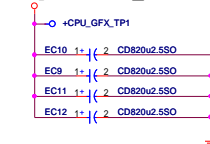
+CPU_VCCP-Decoupling



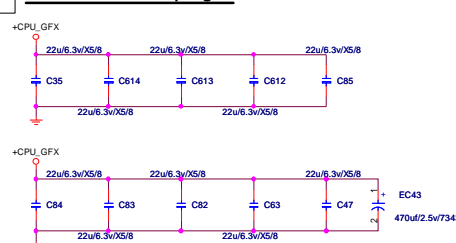
+CPU_GFX



+CPU_GFX +CPU_GFX Output Caps



+CPU_GFX Decoupling



DC-19V_FET DC-19V_FET DC-19V_FET DC-19V_FET DC-19V_FET

C931 C935 C936 C937 C938

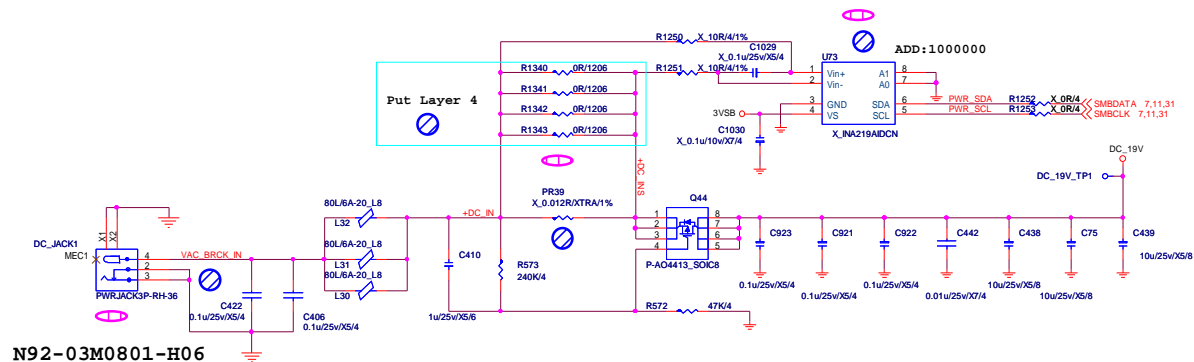
0.1u/25V/X5/4 0.1u/25V/X5/4 0.1u/25V/X5/4 X 0.1u/25V/X5/4 X 0.1u/25V/X5/4



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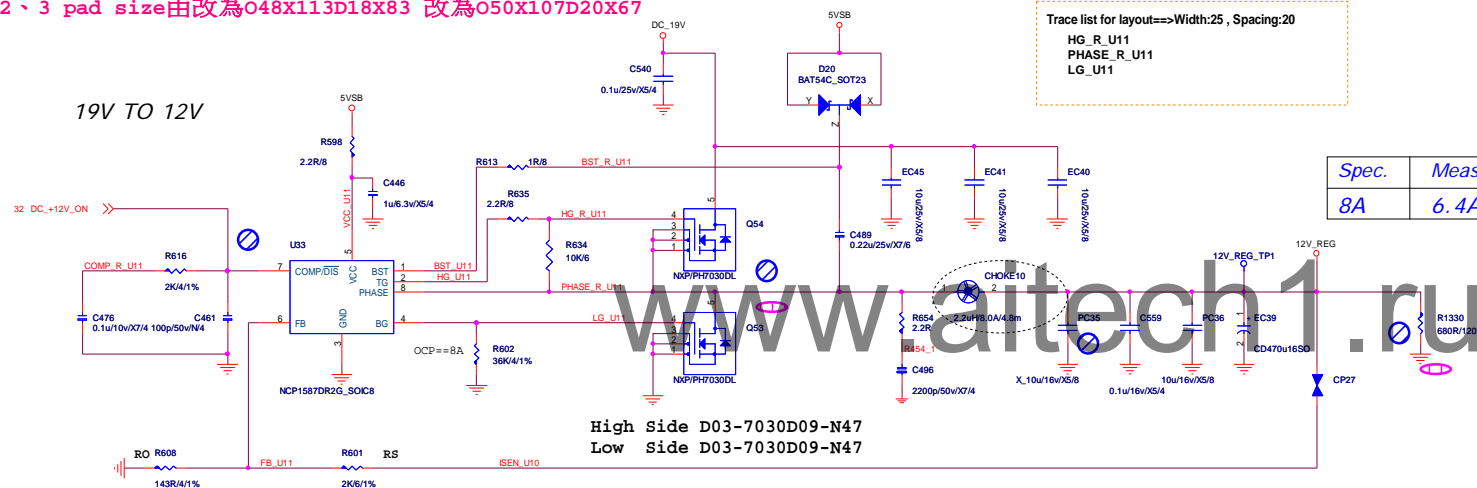


N92-03M0801-H06

請 Layout 重新 更新 Footprint

將零件pin x1、x2 pad size由050X107D20X67改為048X113D18X83，
pin 2、3 pad size由改為048X113D18X83 改為050X107D20X67

19V TO 12V

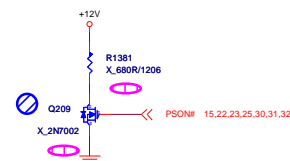
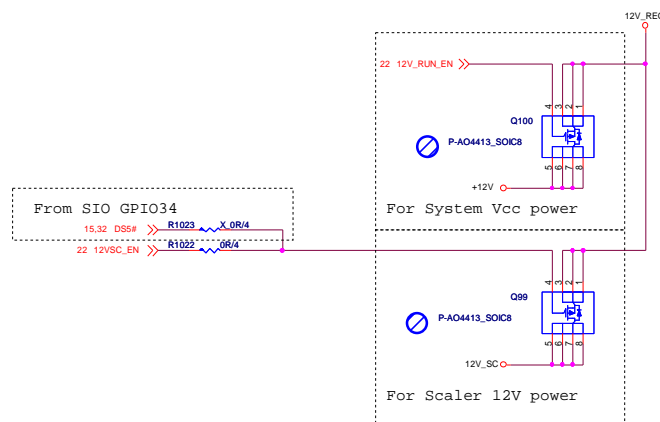


High Side D03-7030D09-N47
Low Side D03-7030D09-N47

I32-0158703-O05

$V_{out} = 0.8 \left(1 + \frac{2K}{143} \right) = 11.989 \text{ Volt}$

DC_19 Volt
+3VALW , +5VALW
VCC3 , VCC5 , 12V_REG , VCC_DDR , VTT_DDR
+8V , VCC1_8 , PCH_1p05
CPU_VTT , +1_5RUN
CPU_SA , VCCP , +CPU_GFX



SBD6 + (USB_CARD_P) / SBD6 - (USB_CARD_N) (Zdiff) is $90\Omega \pm 10\%$
 Maintain at least 20 mils air gap to the edge of the reference plane

CLK - DATA | trace length ≤ 100 mils
 DATA - DATA | trace length ≤ 100 mils
 no more 2 via ; 2 inch (maximum)

MS_SCLK (Pin 37 SP14) & SD_CLK (Pin 22 SD_CLK)
 are impedance are $50\Omega \pm 15\%$

Pin 48(RREF trace width 12 mil)
 trace must far away 48MHz clock trace

+3V_CR trace width 30 mil

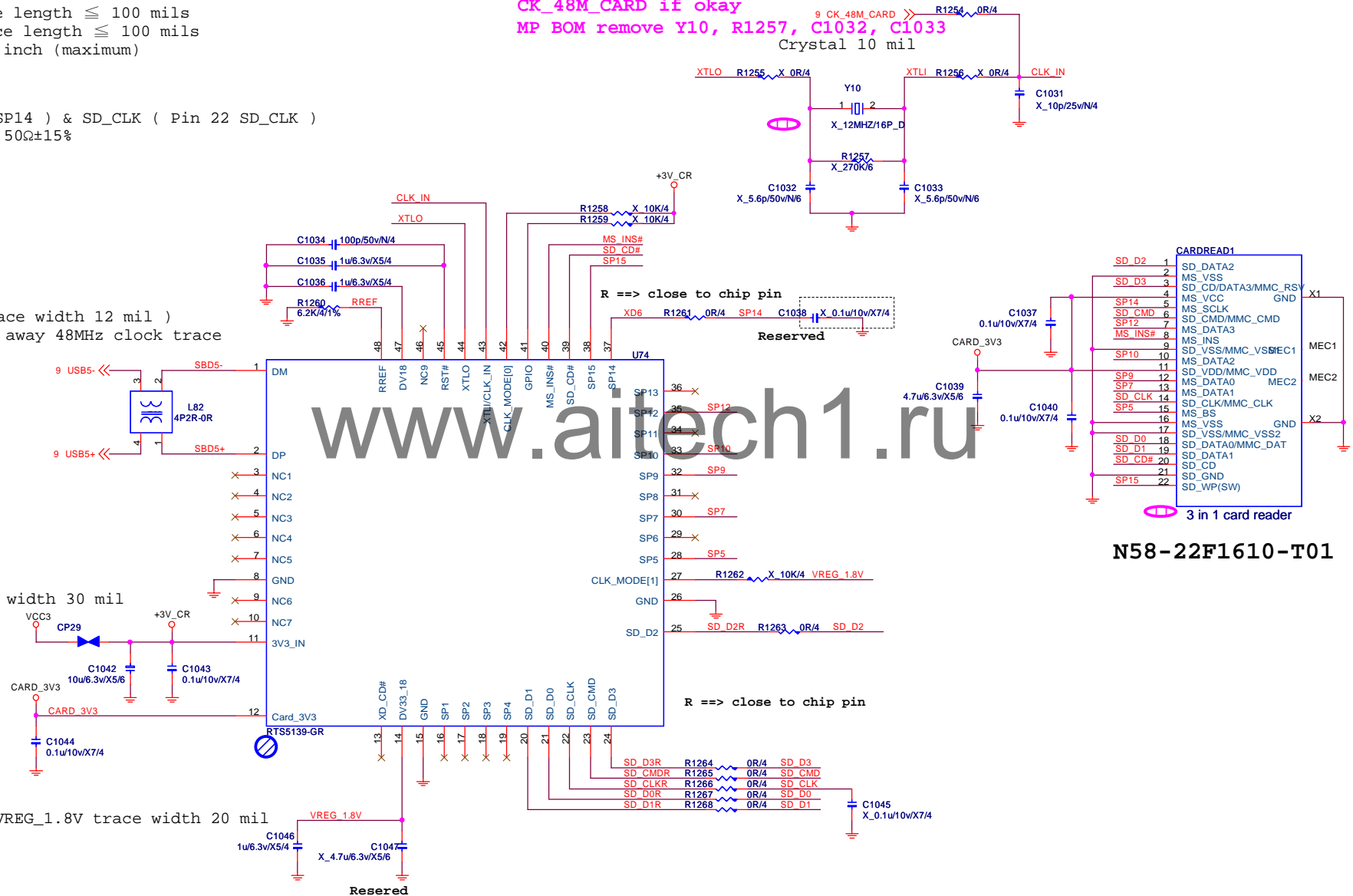
VREG_1.8V trace width 20 mil

CK_48M_CARD if okay

MP BOM remove Y10, R1257, C1032, C1033

Crystal 10 mil

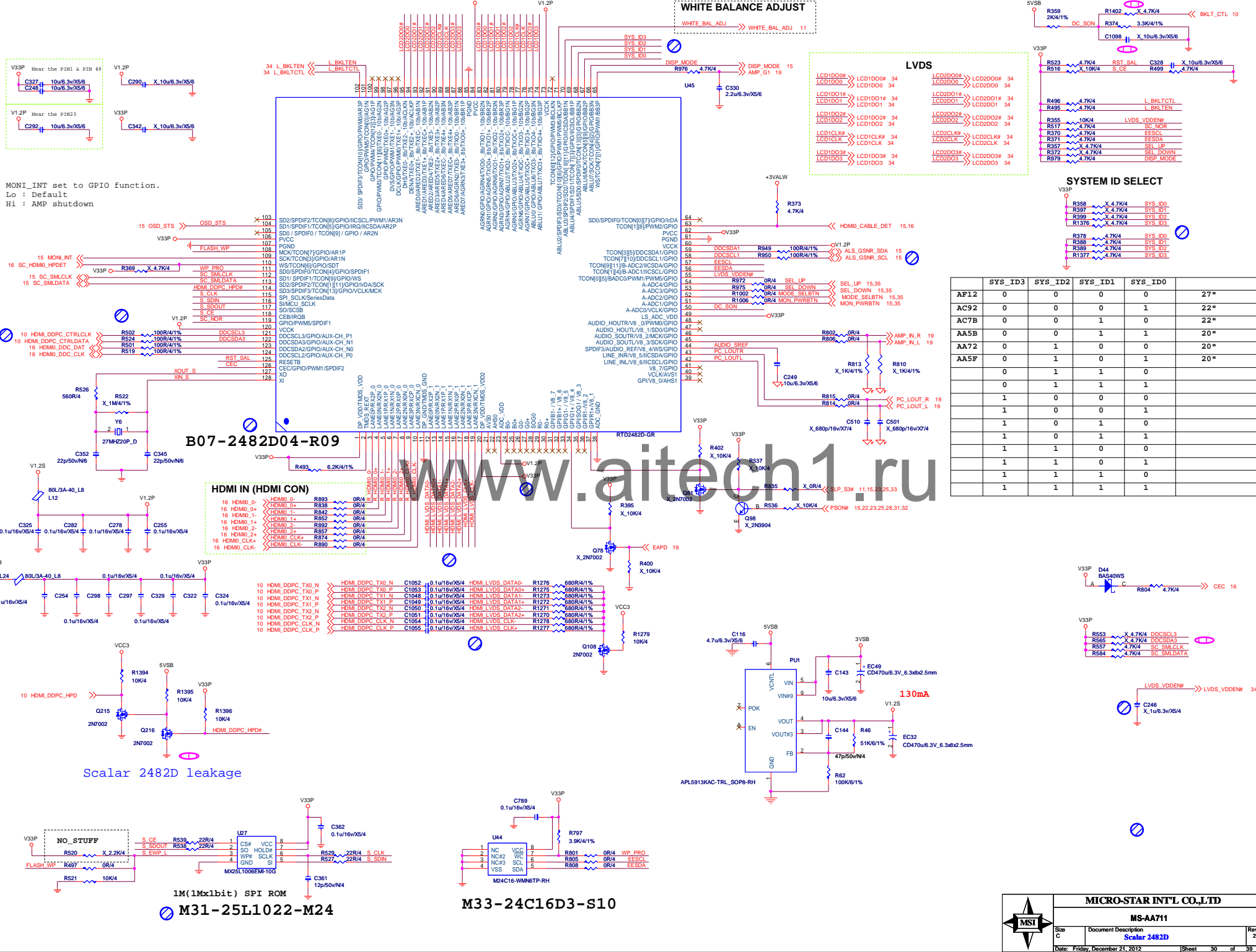
CLK	MODE1 Pin 27 R1262	MODE0 Pin 42 R1258
48MHz	X	X
24MHz	X	1
12MHz (XTAL)	1	1



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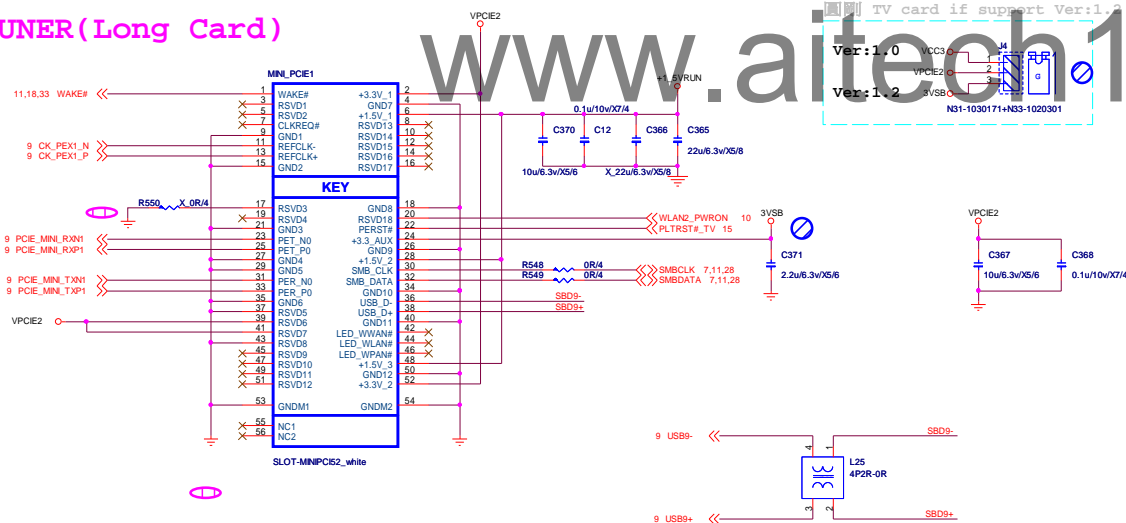
MS-A612

Size	Document Description	Rev
Custom	RT5139 (Card Reader)	2.1
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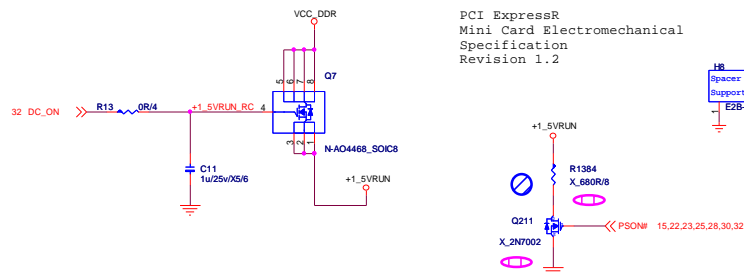


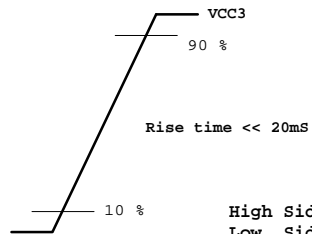
[illegible]

TV TUNER(Long Card)



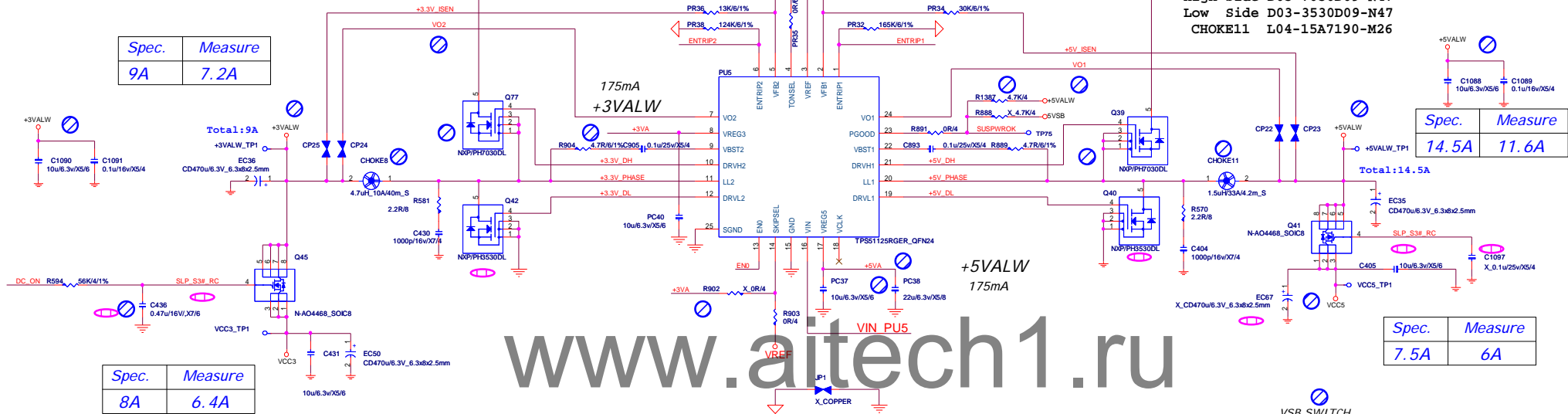
PCI Express®
Mini Card Electromechanical
Specification
Revision 1.2





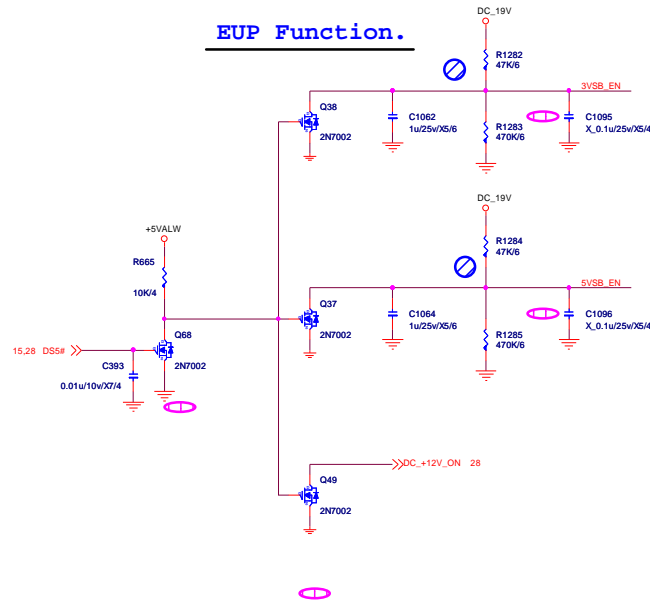
High Side D03-7030D09-N47
Low Side D03-3530D09-N47
CHOKE8 L04-47A7560-M26

Spec.	Measure
9A	7.2A

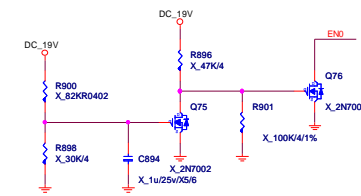


EUP Function.

EN0 open: LDO on and turn on switcher channel



EN0 control circuit



TPS51125

SLU578A-OCTOBER 2007-REVISED NOVEMBER 2007

ELECTRICAL CHARACTERISTICS (continued)
over operating free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Softstart					
tss	Internal SS time	Internal soft start	1.1	1.6	2.1 ms

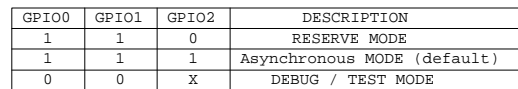
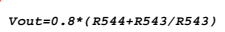
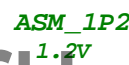
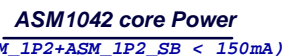
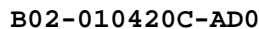


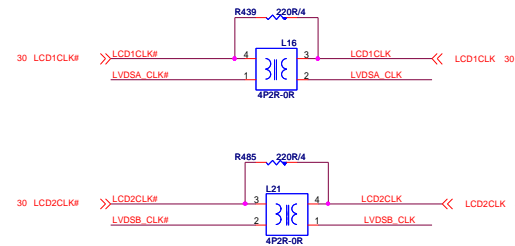
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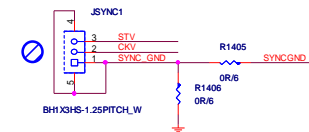
System Power VCC3 / VCC5

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GPIO0 / GPIO1 / GPIO2 INTERNAL PULL-HI



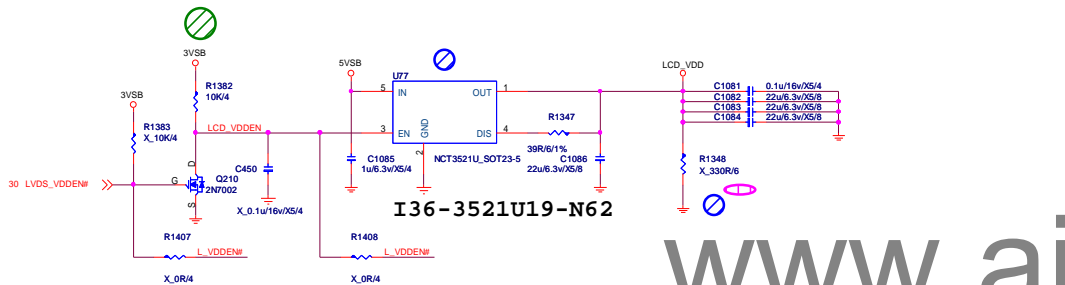
N32-2200410-H06



Pin 37 Reserved for BKLCTL#.

Pin 38 Reserved for LVDS_VDDEN.

Pin 39 Reserved for BKLTEN#.



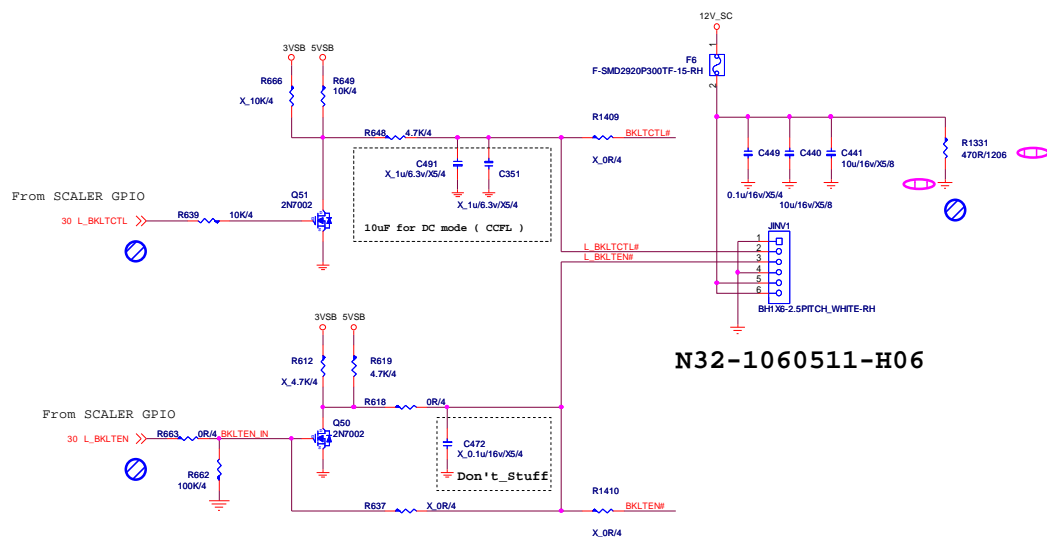
5.26 PCH Display Interfaces

The PCI integrates one Analog, LVDS (mobile only) and three Digital Ports B, C, and D. Each Digital Port can transmit data according to one or more protocols. Digital Port B, C, and D can be configured to drive natively HDMI, DisplayPort, or DVI. Digital Port B also supports Serial Digital Video Out (SDVO) that converts one protocol to another. Digital Port D can be configured to drive natively Embedded DisplayPort (eDP). Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device.

The PCH's Analog Port uses an integrated 340.4 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.

The PCH SDVO port (configured through Digital Port B) is capable of driving a 200 MP/s (Megapixels/second) rate.

Each Digital Port is capable of driving a digital display up to 2560x1600 at 60 Hz using DisplayPort and 1920x1200 at 60 Hz using HDMI, DVI (with reduced blanking).

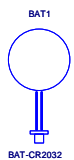
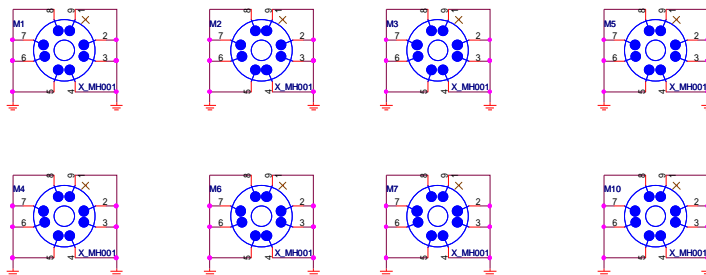
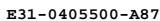


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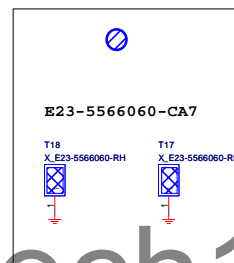
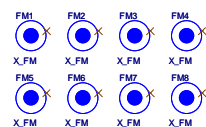
MS-AA711

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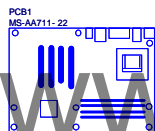
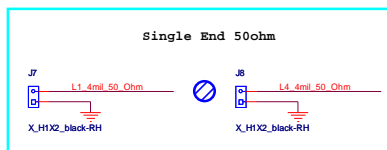
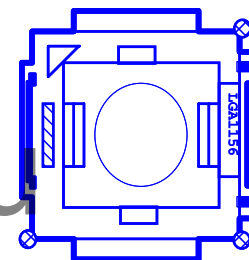
Mounting Holes



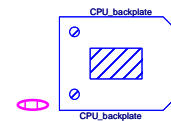
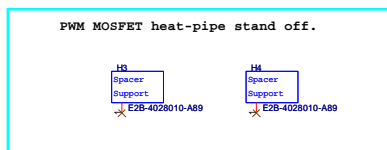
Optical Fiducial Marks-120



CPU SOCKET

CPU_X1
CPU SOCKET

P80-AA71122-E48
P80-AA71122-E55
P80-AA71122-G37



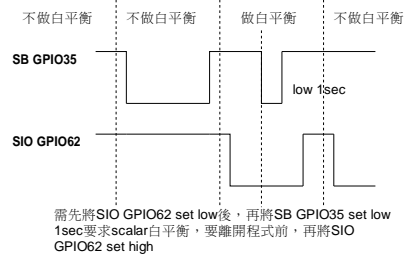
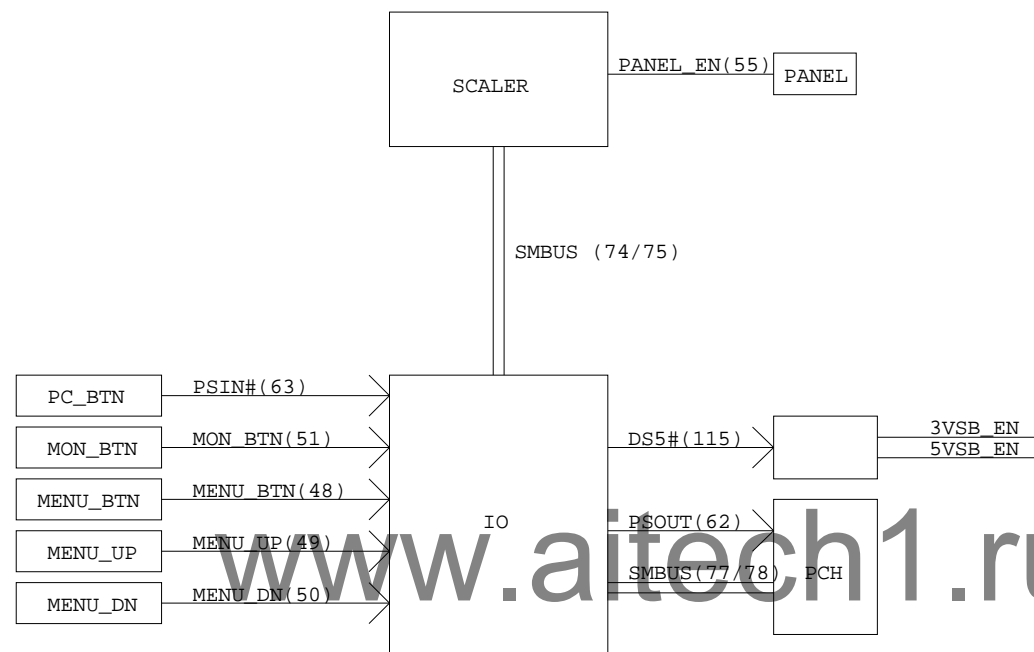
MICRO-STAR INT'L CO.,LTD

MS-AA711

Size C	Document Description Manual parts
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LGA1155 - CPU (65W)	
CPU CORE	- 75A
VCC_DDR	- 4.75A
CPU_SA	- 8.8A
VCC1_8	- 1.5A
CPU_VTT	- 8.5A
+CPU_GFX	- 35A

PCH	
CPU_VTT	- 0.06A
VCC1_8	- 0.179A
PCH_1P05	- 8.16A
VCC3	- 0.355A
3VSB	- 0.13A

REALTEK/RTL8111E-VB	
3VSB -> VDD3	0.17A

HD Audio ALC887	
VCC3	- 0.012A
5VSB -> LDOVDD	- 0.05A

AMP TPA2008	
VCC5 -> PVCC	- 1.5A

DDRIII x2 & TERMINATOR	
VTT_DDR	- 1.2A
VCC_DDR	-8A

SATA HDD /SATA ODD	
VCC5	-3A

(LVDS) LCD PANEL	
VCC5 -> LCD_VDD	- 1.5A
(IRUSH)	-3A

USB 2.0 PORT X4	
5VSB -> SVCC1	- 4A
5VSB -> SVCC2	

USB 3.0 PORT X2	
5VSB -> SVCC4	
5VSB -> SVCC5	- 3A

NCP6151/6131	
CPU CORE	0.25V-1.52V 75A
+CPU_GFX	0.25V-1.52V 35A

NCP5217AMNTXG_QFN14	
VCC_DDR	1.5V 23.71A

NCP5217AMNTXG_QFN14	
NVVDD	Variable 39.37A

NTMFS4841NHT1G_S08	
VCC1_8	1.8V 1.679A

NTMFS4841NHT1G_S08	
CPU_SA	0.925V 8.8A

NTD4809NT4G_DPAK3	
PCH_1P05	1.05V - 8.16A

NCP5217AMNTXG_QFN14	
CPU_VTT	1.05V 21.19A

W83310DG_SOP8	
VTT_DDR	0.75V - 1.2A

N-AO4468_SOIC8	
+1_5VRUN	1.5V - 1A

APL5913KAC-TRL_SOP8	
VCC_1P0	1.05V - 0.6A

Mini PCI-E slot x2	
VCC3	- 2.75A
3VSB	- 2.75A
1.5V -> +1_5VRUN	- 1A

BlueTooth	- 0.5A
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Level Shifter	- 0.15A
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Webcam	- 0.5A
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Card Reader	- 0.3A
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NEC USB3.0	
VCC_1P0	- 0.6A
3VSB -> 3V_DUAL	- 0.11A

+12V CPU & SYS FAN	- 1A
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INVERTER	- 1A
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TI/TPS51120	
VCC5	7.5A
VCC3	7.626A+EDP_VDD
5VSB	14.5A
+5VALW	0.5A
3VSB	8.036A
+3VALW	0.5A

+12V NCP1587DR2G_SOIC8	
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+19V ADAPTER	
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MICRO-STAR INT'L CO.,LTD		
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AIO MS-AA711 Version 2.1 SCHEMATIC HISTORY

Modify from MS-AA711 version 1.1

Rev	Date	Page	Description
2.0	20120705		HDMI In and HDMI Out Location swap. HDMI Out level shift from active change to passive. LVDS from VGA change to DDPC; Scalar from 2482 change to 2482D. EC Crystal from DIP change to SMD. ERP Spec. change to 2013. MOSFET from DPAK change to PPAK reduce thermal. EDI-TENSOR change to new version. LVDS connector turn 180 degree. Card Reader from RTS5159 to RTS5139 Card Reader from 6 in 1 change to 3 in 1. Power Connect change new part. Reserved Power meter circuit. Reserved CMOS Power sequence circuit. Add thermal Trip and Throtting circuit. Add automatic clear COMS circuit.
2.1	20120728	03	Change CPU Socket part number for cost down.
	20120728	07	Add temperature sensor circuit; Change SODIMM socket for cost down.
	20120728	08	Change SODIMM socket for cost down.
	20120728	15	U51 from 8M change to 1M for cost down. R1388 add 33 Ohm for EMI request.
	20120728	20	Reserved F9 for Touch.
	20120728	23	Change PCH_1P05 MOSFET (Q66) for cost down.
	20120728	28	Don't stuff power meter component for cost down. Modify DC_Jack footprint.
	20120728	29	Modify Card Reader Socket footprint.
	20120728	30	Add DDPC HPD circuit. Reserved BKLCTL circuit.
	20120728	31	Change Mini PCIE Slot part number for cost down.
	20120728	32	3VSB_EN and 5VSB_EN reserved C1095, C1096 . Delete R589, R571; Remove EC67. C436 stuff 0.47uf for WebCom issue.
	20120829		1uf / 6.3v from 0603 change to 0402 for cost down. 10uf / 6.3v from 0805 change to 0603 for cost down. 10uf / 16v from 1206 change to 0805 for cost down. 10uf / 25v from 1206 change to 0805 for cost down.
	20120904	08	Power and HDD LED from 330 Ohm change to 2.2K Ohm.
	20120905		Footprint SOT669 change to SOT669_COLAY, for Power team request.
	201201026	11	Y1 change to RALTRON; C221 from 10pF change to 12pF.
	201201026	17	Q213 change main source, and add AVL.
	201201026	9	C266, C267 from 27pF change to 22pF.
	201201026	18	Y7 chnge to TXC.
	201201026	33	Y4 change to TXC.
	201201107	30	Y6 change to TXC.
	201201112		Create New BOM for AA5F.
	201201115	36	LAB1 from 5010 change to 60.
	201201218	10	Add GPIO16 for BIOS.

AIO MS-AA711 Version 2.2

Modify from MS-AA711 version 2.1

Rev	Date	Page	Description
2.2	20121218	10	Add GPIO16 for BIOS setting.
2.2	20121218	24	Add R1411 avoid floating.
2.2	20121218	33	ESD change to for 3.0 spec.
2.2	20121218	34	LVDS1 from FPC change to wired.

MP BOM remove JSYNC1 related component.

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